JEDEC STANDARD

The Measurement of Small-Signal VHF-UHF Transistor Admittance Parameters

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EIA STANDARD

for

THE MEASUREMENT OF SMALL-SIGNAL VHF-UHF TRANSISTOR ADMITTANCE PARAMETERS

ELECTRONIC INDUSTRIES ASSOCIATION
STANDARD RS-372

Formulated by

JEDEC Semiconductor Device Council

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STANDARD FOR THE MEASUREMENT OF SMALL-SIGNAL VHF-UHF TRANSISTOR ADMITTANCE PARAMETERS

(From Standards Proposal No. 1029, formulated under the cognizance of the JEDEC JS-9 Committee on Low Power Transistors.)

1. DEFINITIONS

1.1 Definition of the admittance parameters

Given a two-port network as shown in Figure 1, where v_1, i_1, v_2, and i_2 represent the voltage and the current at ports one and two respectively, the admittance parameters may be defined as the elements of the matrix

$$Y = \begin{vmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{vmatrix} \quad (1)$$

associated with the linear equations

$$i_1 = y_{11}v_1 + y_{12}v_2 , \quad (2)$$

and

$$i_2 = y_{21}v_1 + y_{22}v_2 . \quad (3)$$

Each of the above parameters may be individually defined as follows:

y_{11} is the driven-point admittance at port one with port two short-circuited, i.e.,

$$y_{11} = \left.\frac{i_1}{v_1}\right|_{v_2 = 0} \quad (4)$$

y_{12} is the reverse transadmittance with port one short-circuited, i.e.,

$$y_{12} = \left.\frac{i_1}{v_2}\right|_{v_1 = 0} \quad (5)$$

y_{21} is the forward transadmittance with port two short-circuited, i.e.,

$$y_{21} = \left. \frac{i_2}{v_1} \right|_{v_2 = 0} \tag{6}$$

y_{22} is the driving-point admittance at port two with port one short-circuited, i.e.,

$$y_{22} = \left. \frac{i_2}{v_2} \right|_{v_1 = 0} \tag{7}$$

The admittance parameters of transistors are also commonly represented by the following symbols:

y_{11} is represented by y_{ix},
y_{12} is represented by y_{rx},
y_{21} is represented by y_{fx},
y_{22} is represented by y_{ox},

where x is replaced by e, b, or c for bipolar transistors in common-emitter, common-base and common-collector configuration respectively; and by d, g, or s for field-effect transistors in common-drain, common-gate or common-source configuration respectively.

1.2 Definition of small-signal conditions

Transistors are essentially non-linear devices which, for sufficiently small applied signals, behave as linear two-ports.

Small-signal conditions may, therefore, be defined as the values of the voltage and current at ports one and two, below which the transistor may be considered a linear two-port.

For practical applications, the following definition will be used: Small-signal conditions are satisfied when a reduction of 50% in the amplitudes of v_1, i_1, v_2 or i_2 will not result in a variation of the ratio defined by (4), (5), (6) or (7) of more than 1%.*

*All asterisks in this document refer to the following footnote:

The numerical values quoted have been agreed upon by the JS-9 JEDEC committee as those representing a practical compromise between the usual requirements of circuit design applications of admittance parameters and the measurement technology at the time of writing this document.

1.3 Definition of the transistor terminals

In standard single-ended axial-lead transistor packages, the transistor terminals for the purposes of this standard are the points on said leads at a distance of 1.5 mm (0.06") from the seating plane of the transistor package, (see Fig. 2) which points define the reference plane of the transistor terminals.

In special packages not provided with leads (e.g. strip-line or coaxial packages), the transistor terminals must be specifically defined for each particular package.

2. MOUNTS FOR SINGLE-ENDED AXIAL-LEAD TRANSISTORS

The transistor mount must satisfy the following requirements:

a – It shall have two well-shielded terminals, preferably coaxial, to which ports one and two of the transistor-under-test are connected.

b – It shall have two ground connections to which the common terminal and a possible shield of the transistor package are connected.

c – The magnitude of the transfer susceptance between the two shielded terminals (when no device is inserted in the mount) shall be less than 1) 5%* of the magnitude of the reverse transfer susceptance of the transistor-under-test, or 2) less than that susceptance corresponding to a capacitance of 0.001 pF,* whichever is greater.

d – The shielded terminals shall be designed to eliminate the high-frequency effects of that part of each lead extending from the transistor terminal defined in 1.3 above to the physical extremity of said lead. This is normally achieved by the use of tubular inputs in which the transistor leads are inserted.

e – The location of the reference plane of the shielded terminals shall be known within less than ± one thousandth of the wave length* at the test frequency.

f – Repeatable low-resistance electrical contact between the transistor leads and the terminals of the mount shall be made within 0.5 mm (0.02")* of the intended contact points.

g – No portion of the mount shall extend beyond the reference plane defined in paragraph (e) above.

h – No insulating materials shall be placed in the air-gap between the seating plane of the transistor package and the reference plane of the transistor mount (see Fig. 2).

i – When the transistor mount consists of constant-impedance transmission lines, the VSWR introduced by the transistor mount shall be less than $(1.01 + 0.03\ f_{GHz})$* with respect to the characteristic impedance of the system to which the transistor mount is connected. The expression f_{GHz} represents the test frequency in gigahertz.

j – When transmission lines are used to make the connection between the transistor and the measuring system, a d-c blocked damping resistor may be connected provided the connection is made within 0.5 mm (0.02")* of the reference plane of the shielded terminals if a short circuit is effectively reflected at this terminal.

3. THE MEASURING SYSTEM FOR ADMITTANCE PARAMETERS

3.1 General

The measuring system must provide a means for applying bias to the transistor under test. The bias system must be such as not to influence the accuracy of the measurements.

The signal applied by the measuring system to the transistor must be sufficiently small to satisfy the "small-signal conditions" defined in 1.2. In addition, any spurious signals which might appear at the transistor terminals, and in particular, the local oscillator feedthrough when a superheterodyne receiver is used, must be kept at least 20 dB* below the specified small-signal conditions.

Ideally, the measurement of an admittance parameter would require a perfect voltage source at one port and a perfect short circuit at the other. Such requirements cannot be simultaneously fulfilled in practice; measurements have to be made with finite source impedances or load admittances, or both. The schematic diagram of Fig. 3 illustrates the general case and the specifications are given below.

3.2 Source impedance and load admittance

The effective impedance of the source and the effective admittance of the load applied at the specified terminals of the transistor-under-test must satisfy the following conditions:

$$|Z_S| \cdot y_M < \underline{0.1}^*, \quad (8)$$

$$|Z_S| \cdot |y_a| < \underline{0.1}^*, \quad (9)$$

$$|Z_S| \cdot |y_b| < \underline{0.1}^*, \quad (10)$$

$$y_M / |Y_L| < \underline{0.1}^*, \quad (11)$$

where:

Z_S = source impedance,

Y_L = load admittance,

$y_a = (y_{12}\, y_{21})/(y_{22} + Y_L)$,

$y_b = (y_{12}\, y_{21})/(y_{11} + Y_L)$,

y_M = maximum possible value of the magnitude of any of the four admittance parameters.

3.3 Correction formulas

For more accurate results, the correction formulas given below and derived in the appendix may be used.

$$y_{11} = y'_{11}[1 + (y_a/y'_{11} + Z_S y'_{11})], \quad (12)$$

$$y_{22} = y'_{22}[1 + (y_b/y'_{22} + Z_S y'_{22})], \quad (13)$$

$$y_{12} = y'_{12}[1 + (y_{11}/Y_L + Z_S y_{22})], \quad (14)$$

$$y_{21} = y'_{21}[1 + (y_{22}/Y_L + Z_S y_{11})], \quad (15)$$

where the primed letters represent the measured values of the admittance parameters whereas the unprimed letters represent the true values of the admittance parameters.

The values of the source impedance Z_S and of the load admittance Y_L must be known within ± 10%.*

It is recognized that since Y_a and Y_b contain the true values, successive approximations may be necessary; however, in most cases the true values may be replaced by the measured values in calculating Y_a and Y_b.

3.4 Transmission lines

Transmission lines may be used to make the connection between the transistor mount and the measuring system. These lines may include adjustable-length sections and may also be used for impedance transformations. However, the VSWR created by any residual reflections in the lines must not exceed $(1.025 + 0.005\ f_{GHz})$* where f_{GHz} represents the test frequency expressed in gigahertz. Also, the errors in the measured parameters caused by losses in the lines must be less than 10%.* If these errors exceed 1%* appropriate corrections should be made.

APPENDIX

1. Derivation of formulas (12) and (13)

Let the source driving the transistor-under-test be characterized by the voltage v_S and by the impedance Z_S (see Fig. 3). The value of y'_{11} may be expressed by

$$y'_{11} = \frac{i_1}{v_S} = \frac{1}{Z_S + 1/(y_{11} - y_a)}, \tag{16}$$

which, solved for y_{11}, yields

$$y_{11} = y'_{11} \frac{1 - Z_S y_a + y_a/y'_{11}}{1 - Z_S y'_{11}} . \tag{17}$$

If condition (8) is taken into consideration, the above equation can be modified to give

$$y_{11} \approx y'_{11} \left\{1 + [y_a/y'_{11} + + Z_S y'_{11}(1 - Z_S y_a)]\right\} . \tag{18}$$

However, because of condition (9) the term $Z_S y_a$ can be neglected, and (18) reduces to

$$y_{11} \approx y'_{11} \; [1 + (y_a/y'_{11} + Z_S y'_{11})]. \tag{19}$$

Formula (13) may be obtained by a similar derivation.

2. Derivation of formulas (14) and (15)

The value of y'_{21} is given by

$$y'_{21} = - Y_L v_2/v_S, \tag{20}$$

and the ratios v_2/v_1 and v_1/v_S by

$$\frac{v_2}{v_1} = - \frac{y_{21}}{y_{22} + Y_L}, \tag{21}$$

and

$$\frac{v_1}{v_S} = \frac{1}{1 + Z_S(y_{11} - Z_S y_a)} . \tag{22}$$

Combining (20), (21) and (22) yields

$$y_{21} = y'_{21} \; (1 + y_{22}/Y_L)\,(1 + Z_S y_{11} - Z_S y_a). \tag{23}$$

Substituting the values of y_a in Eq. (23) and rearranging the terms yields

$$y_{21} = y'_{21} \left\{ 1 + \frac{y_{22}}{Y_L} + Z_S Y_{11} [1 + (y_{22} - \frac{y_{12} y_{21}}{y_{11}})/Y_L] \right\} . \qquad (24)$$

Since the absolute value of the expression

$$(y_{22} - \frac{y_{12} y_{21}}{y_{11}})/Y_L \qquad (25)$$

is less than $2y_M/|Y_L|$ and consequently less than 0.2, it can be neglected with respect to unity in Eq. (24), which after this simplification, reduces to

$$y_{21} \approx y'_{21} [1 + (y_{22}/Y_L + Z_S y_{11})] . \qquad (26)$$

Formula (14) may be obtained by a similar derivation.

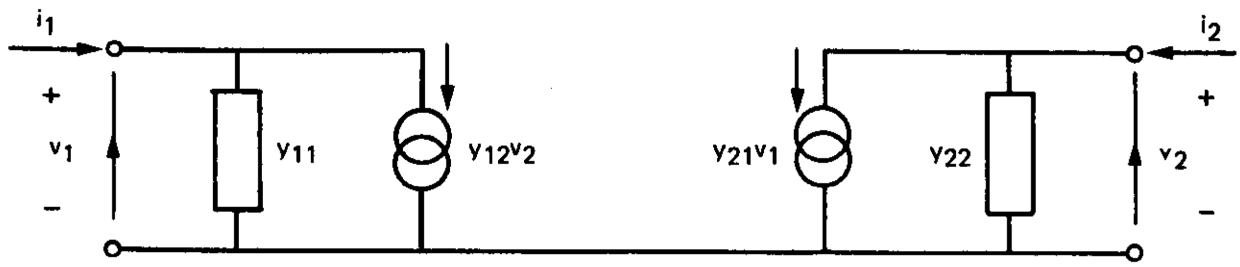

Fig. 1 – Admittance parameters of transistor-under-test

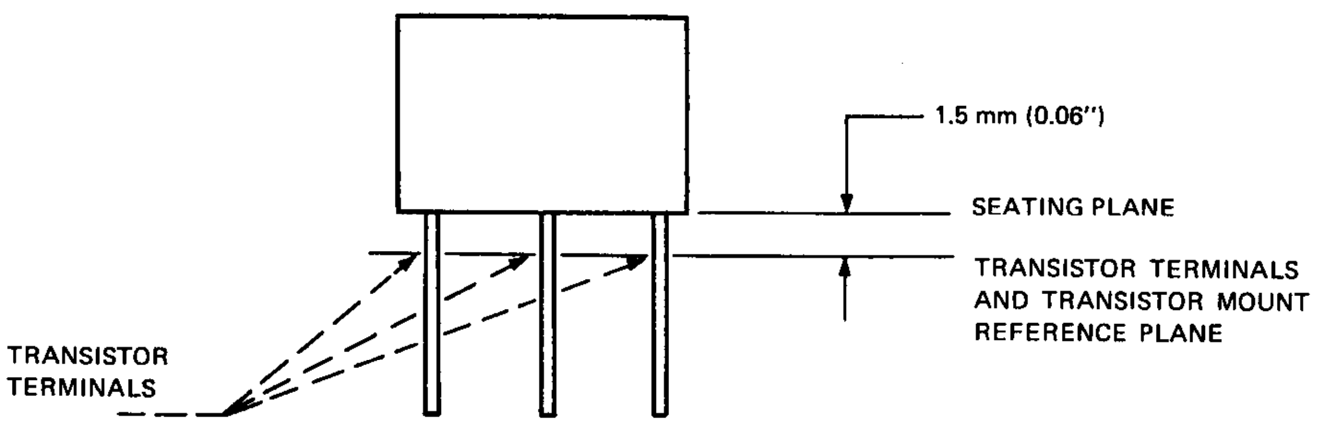

Fig. 2 – Transistor Terminals

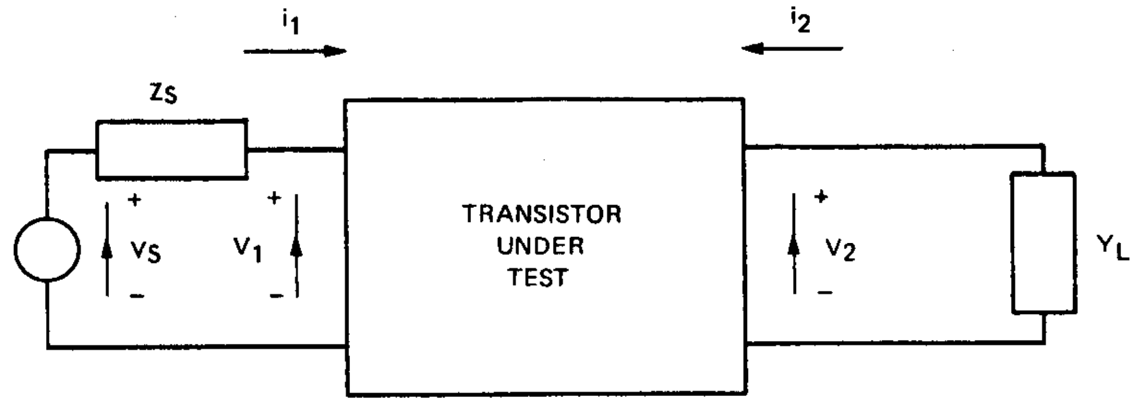

Fig. 3a – Source impedance and load admittance shown for Y_{11} and Y_{21}

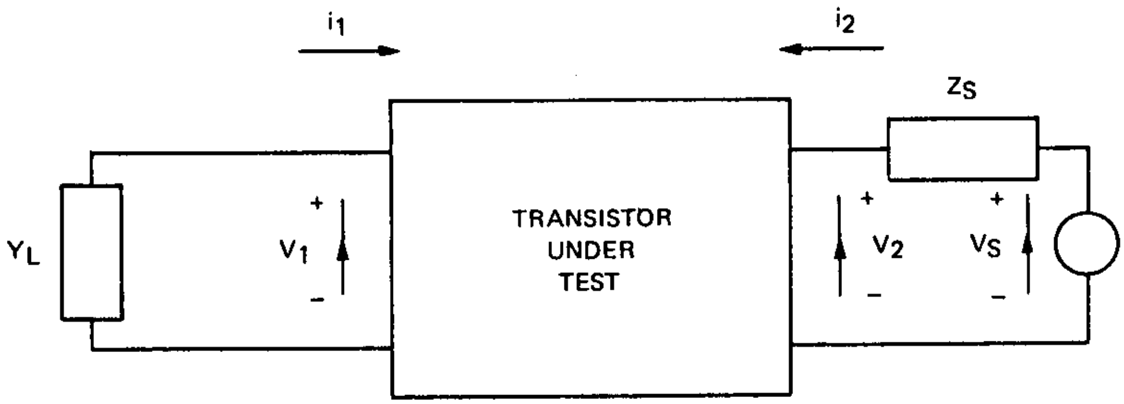

Fig. 3b – Source impedance and load admittance shown for Y_{12} and Y_{22}

RELATED EIA STANDARDS

In addition to this Standard, the following EIA Standards are available on measurements of semiconductor devices in VHF and UHF applications:

RS-306	Standards for Measurement of Small Signal HF, VHF and UHF Power Gain Transistors (NEMA Publication No. SK 506-1965)	$ .60
RS-311	Measurement of Transistor Noise Figure at HF and VHF (NEMA Publication No. SK 509-1965)	$1.00
RS-371	The Measurement of Small Signal VHF-UHF Transistor Short-Circuit Forward Current Transfer Ratio	$1.40

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